Al Mansoura University

Faculty of Engineering

Electronics and Communications Dept.

2nd Year Students

Logic Circuit 2

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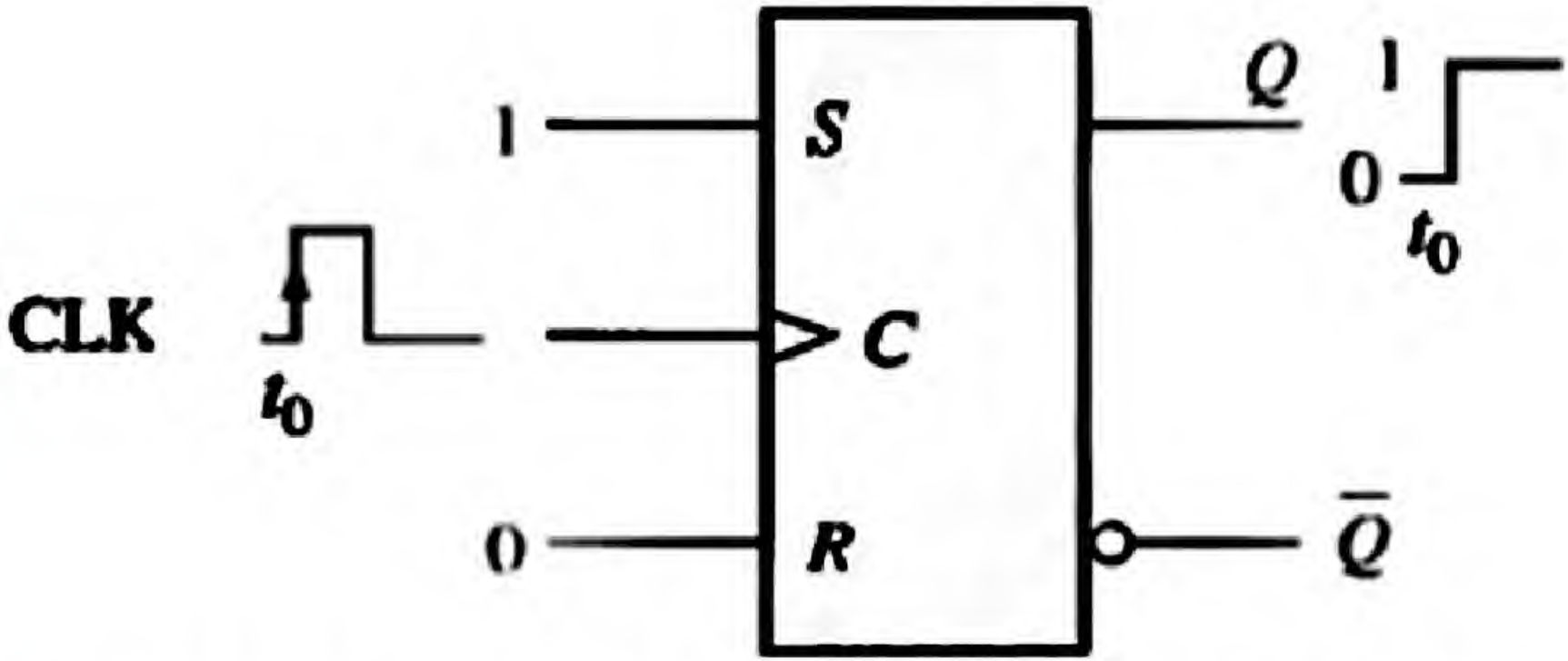
Chapter 1: Latches

Lecture No. 2

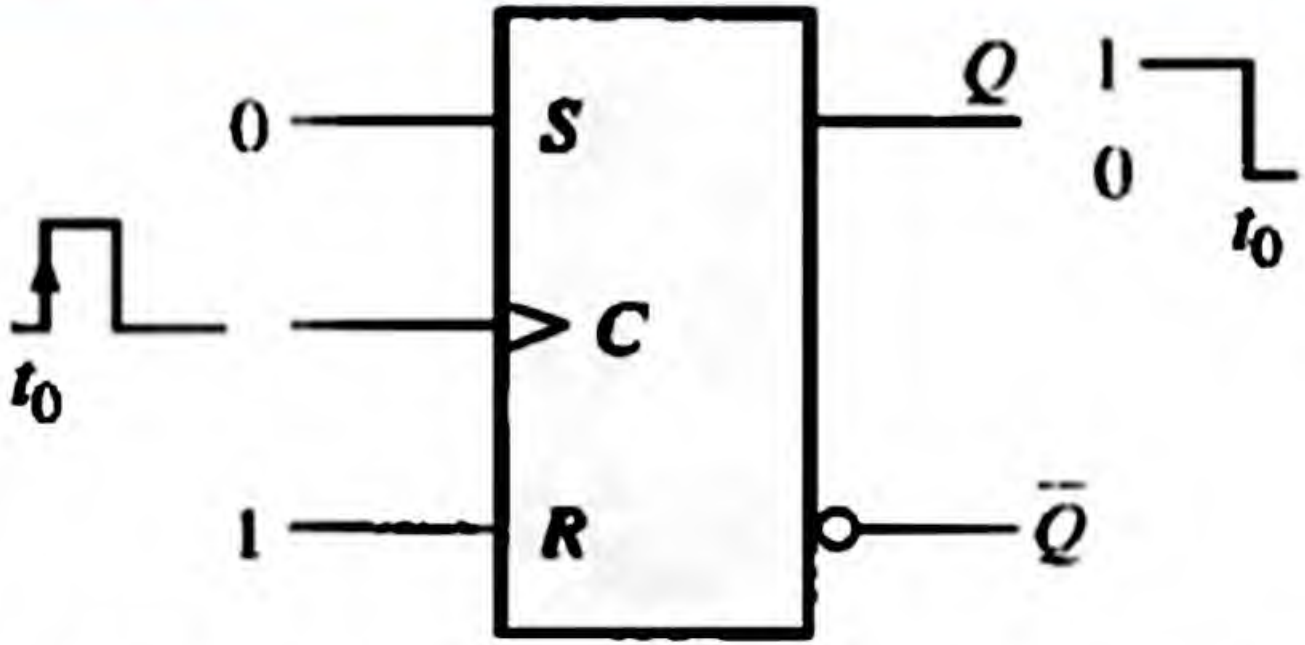
1.6- The Edge-Triggered S-R Flip-Flop.

- ✓ The S and R inputs of the S-R flip-flop are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse.
- ✓ When S is HIGH and R is LOW, the Q output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET.



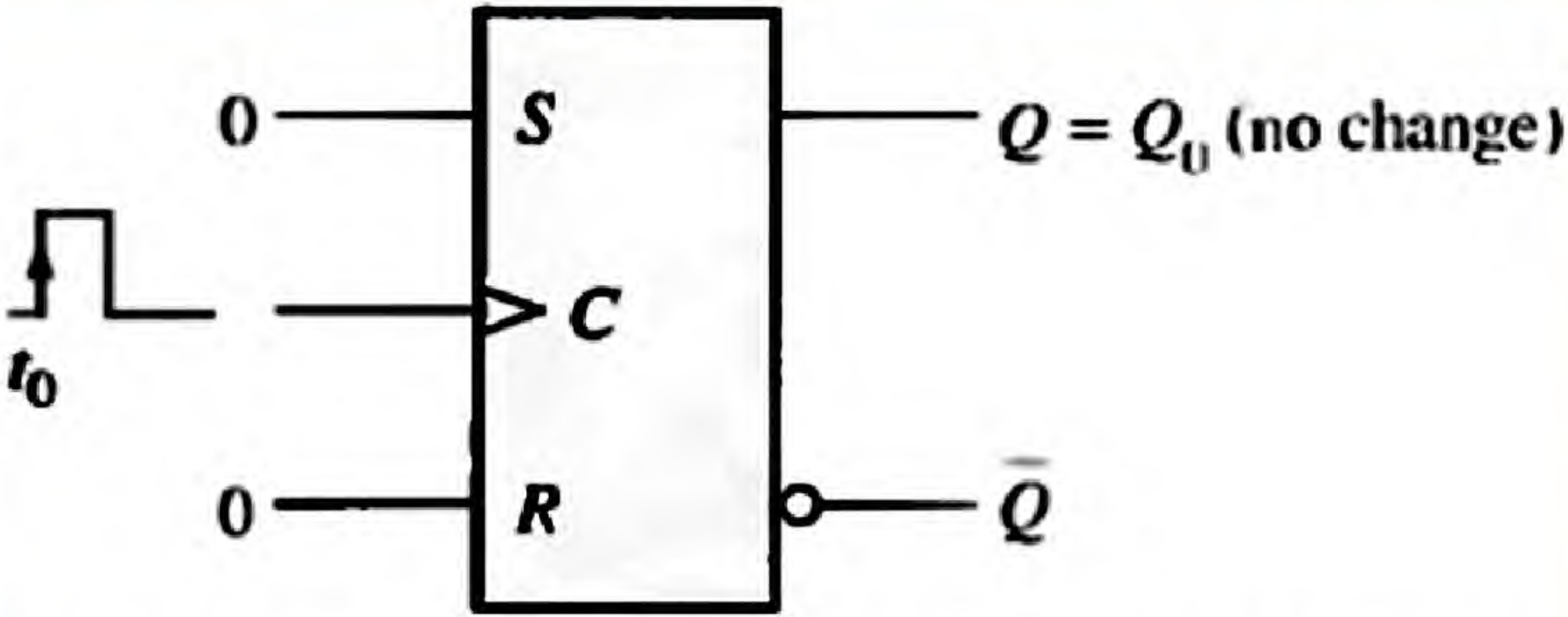
(a) $S = 1, R = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

✓ When S is LOW and R is HIGH, the Q output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET



(b) $S = 0$. $R = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

✓ When both S and R are LOW, the output does not change from its prior state.



(c) $S = 0$, $R = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

✓ An invalid condition exists when both S and R are HIGH.

Table (1.2) Truth table for a positive edge triggered S-R flip-flop.

INPUTS			OUTPUTS		
S	R	CLK	Q	$\overline{Q}$	COMMENTS
0	0	X	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid

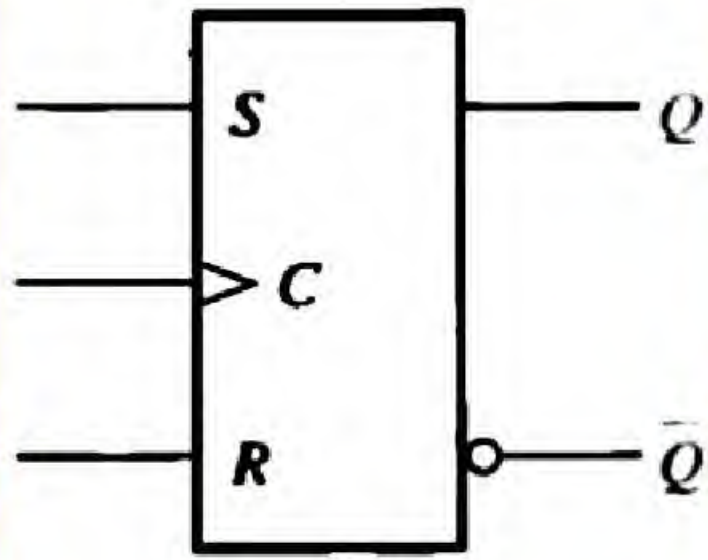
↑ = clock transition LOW to HIGH

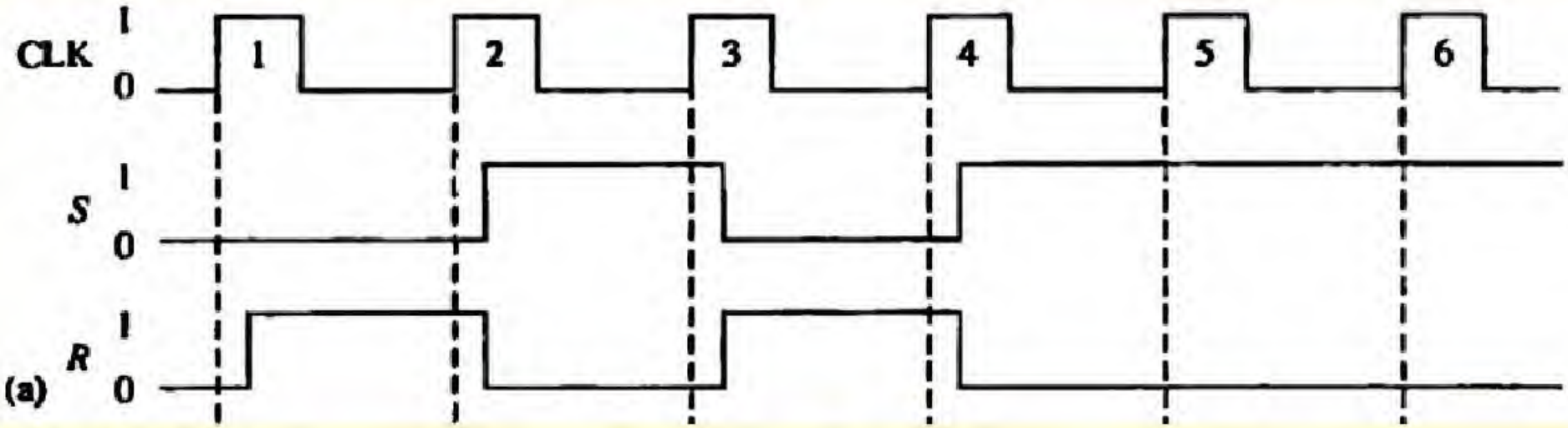
X = irrelevant ("don't care")

Q_0 = output level prior to clock transition

- ✓ The operation and truth table for a negative edge-triggered S-R flip-flop are the same as those for a positive edge-triggered device except that the falling edge of the clock pulse is the triggering edge.

Example 1.4: Determine the Q and $\overline{Q}$ output waveforms of the flip-flop shown in the Figure for the S, R, and CLK inputs shown in the Figure. Assume that the positive edge-triggered flip-flop is initially RESET.


S
C
R
Q
$\bar{Q}$


CLK
S
R
1
0
1
2
3
4
5
6
(a)

Solution:

State Table.

CLK No.	S	R	State	Q	$\overline{Q}$
1	0	0	NC	0	1
2	0	1	Reset	0	1
3	1	0	Set	1	0
4	0	1	Reset	0	1
5	1	0	Set	1	0
6	1	0	Set	1	0

1. At clock pulse 1, S is LOW and R is LOW, so Q does not change, NC.

2. At clock pulse 2, S is LOW and R is HIGH, so Q remains LOW (RESET).

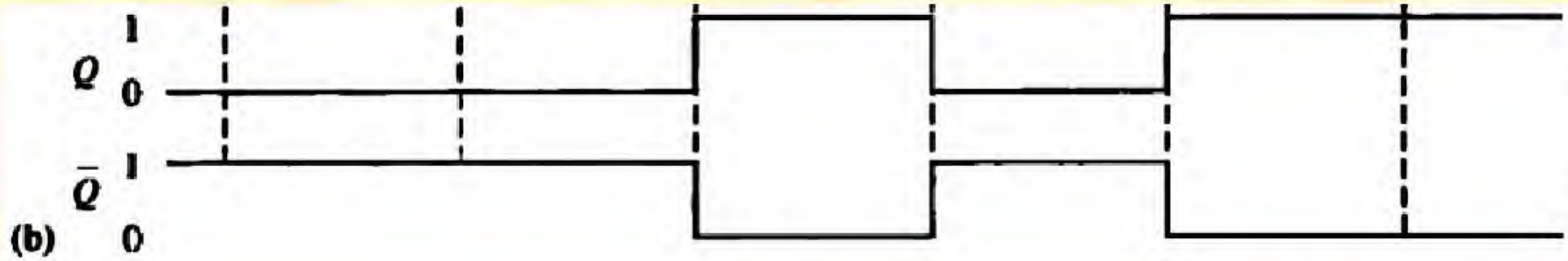
3. At clock pulse 3, S is HIGH and R is LOW, so Q goes HIGH (SET).

4. At clock pulse 4, S is LOW and R is HIGH, so Q goes LOW (RESET).

5. At clock pulse 5, S is HIGH and R is LOW, so Q goes HIGH (SET).

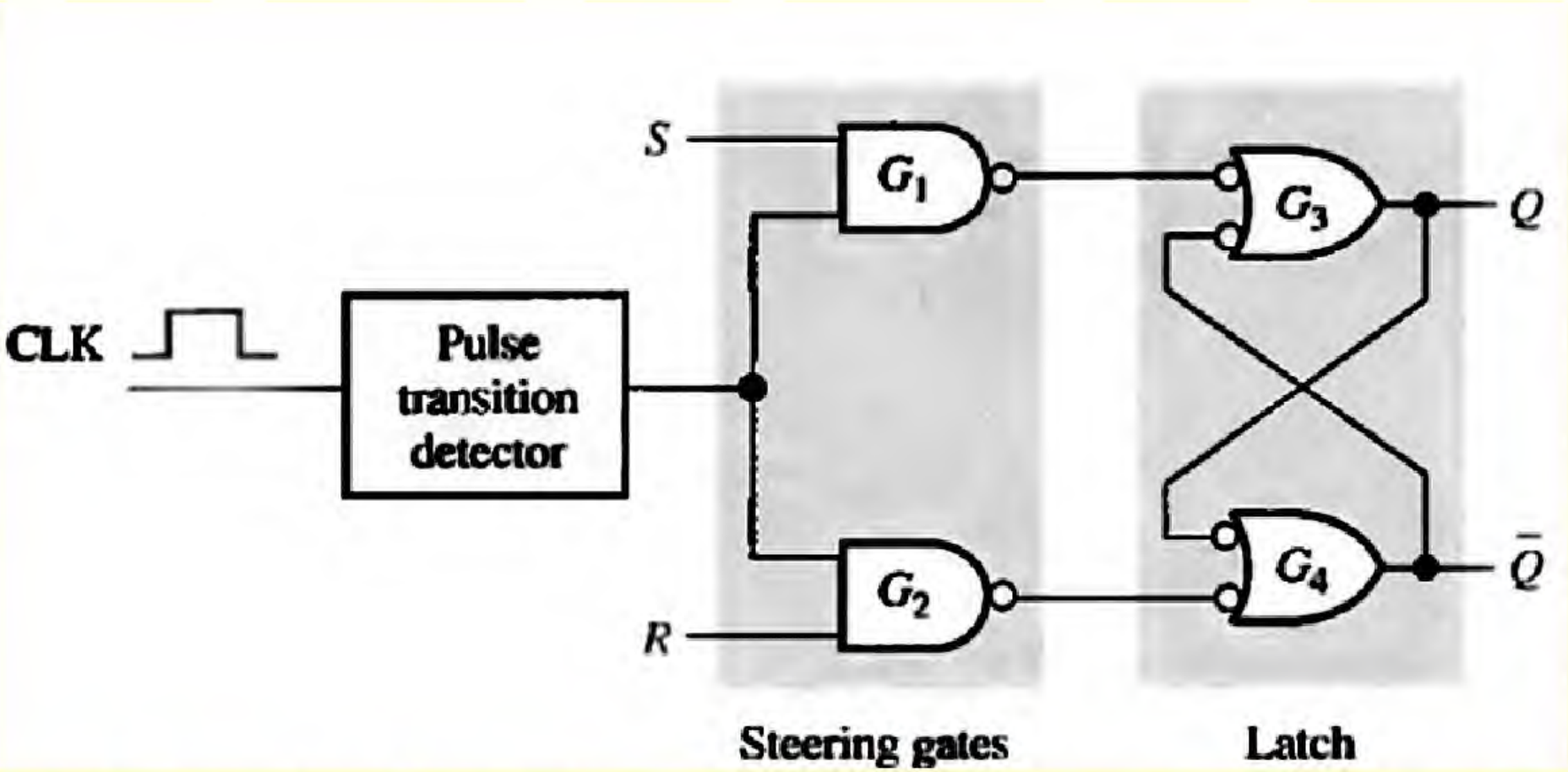
6. At clock pulse 6, S is HIGH and R is LOW, so Q stays HIGH.

✓ Once Q is determined, $\overline{Q}$ is easily found since it is simply the complement of Q. The resulting waveform, for Q and $\overline{Q}$ are shown in the Figure.



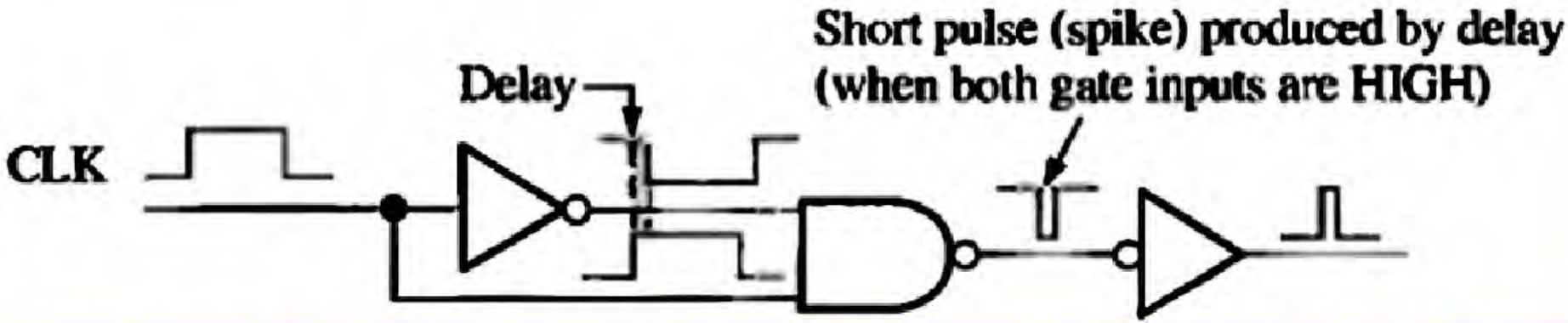
1.6.1-A Method of Edge-Triggering.

- ✓ A simplified implementation of an edge-triggered S-R flip-flop is illustrated in Figure 1-8(a) and is used to demonstrate the concept of edge-triggering.
- ✓ The circuit in Figure 1.8 (a) is partitioned into two sections, one labeled Steering gates and the other labeled Latch.
- ✓ The steeling gates direct, or steer, the clock spike either to the input to gate G_3 or to the input to gate G_4, depending on the state of the S and R inputs.



(a) A simplified logic diagram for a positive edge-triggered S-R flip-flop

✓ One basic type of pulse transition detector is shown in Figure 1.8 (b).



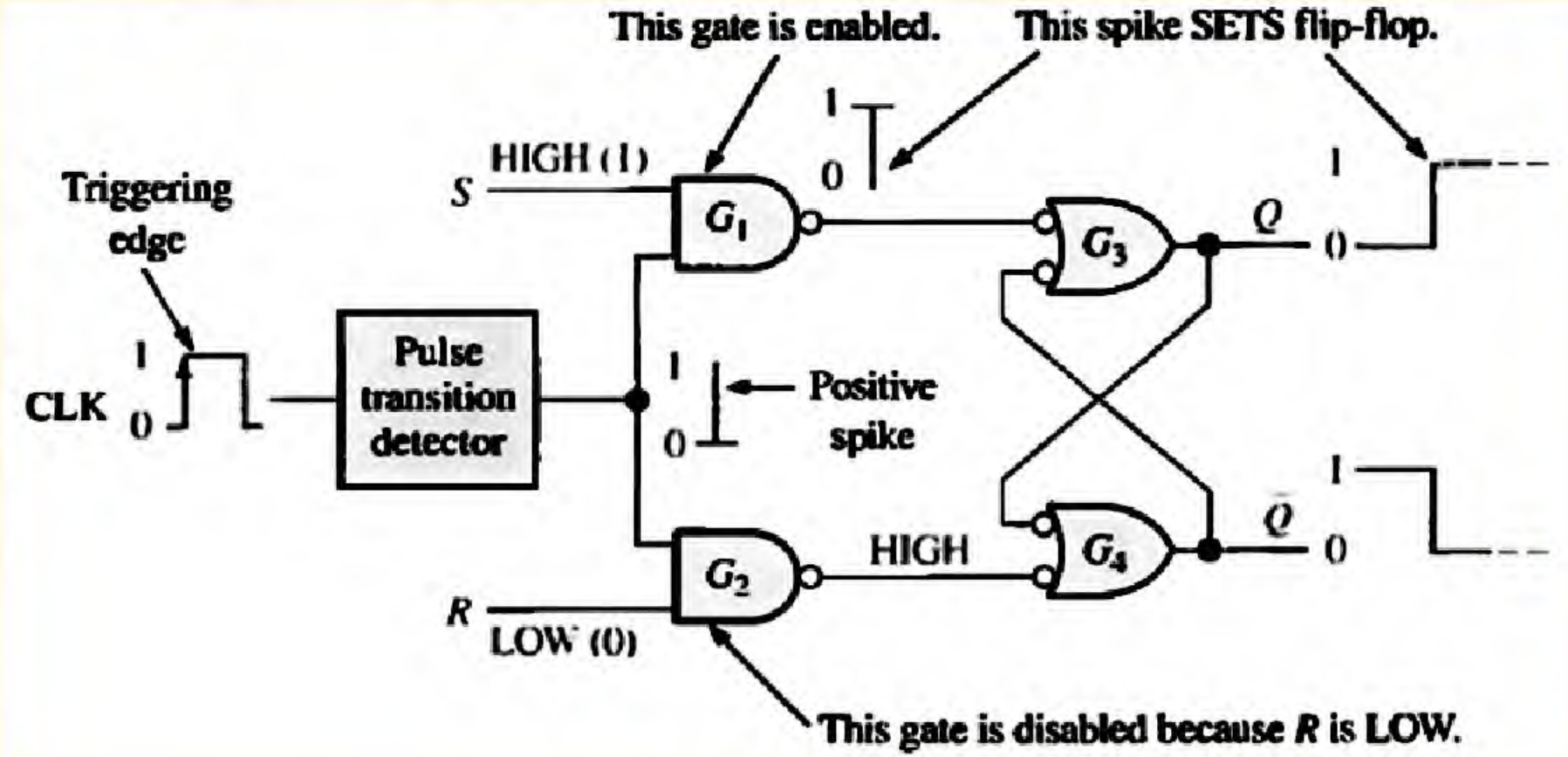
(b) A type of pulse transition detector Figure 1.8

✓ As you can see, there is a small delay on one input to the NAND gate so that the inverted clock pulse arrives at the gate input a few nanoseconds after the true clock pulse.

- ✓ This circuit produces a very short-duration spike on the positive-going transition of the clock pulse.
- ✓ In a negative edge-triggered flip-flop the clock pulse is inverted first, thus producing a narrow spike on the negative-going edge.
- ✓ To understand the operation of this flip-flop, begin with the assumptions that it is in the RESET state (Q = 0) and that the S, R, and CLK inputs are all LOW. For this condition, the outputs of gate G_1 and gate G_2 are both HIGH.

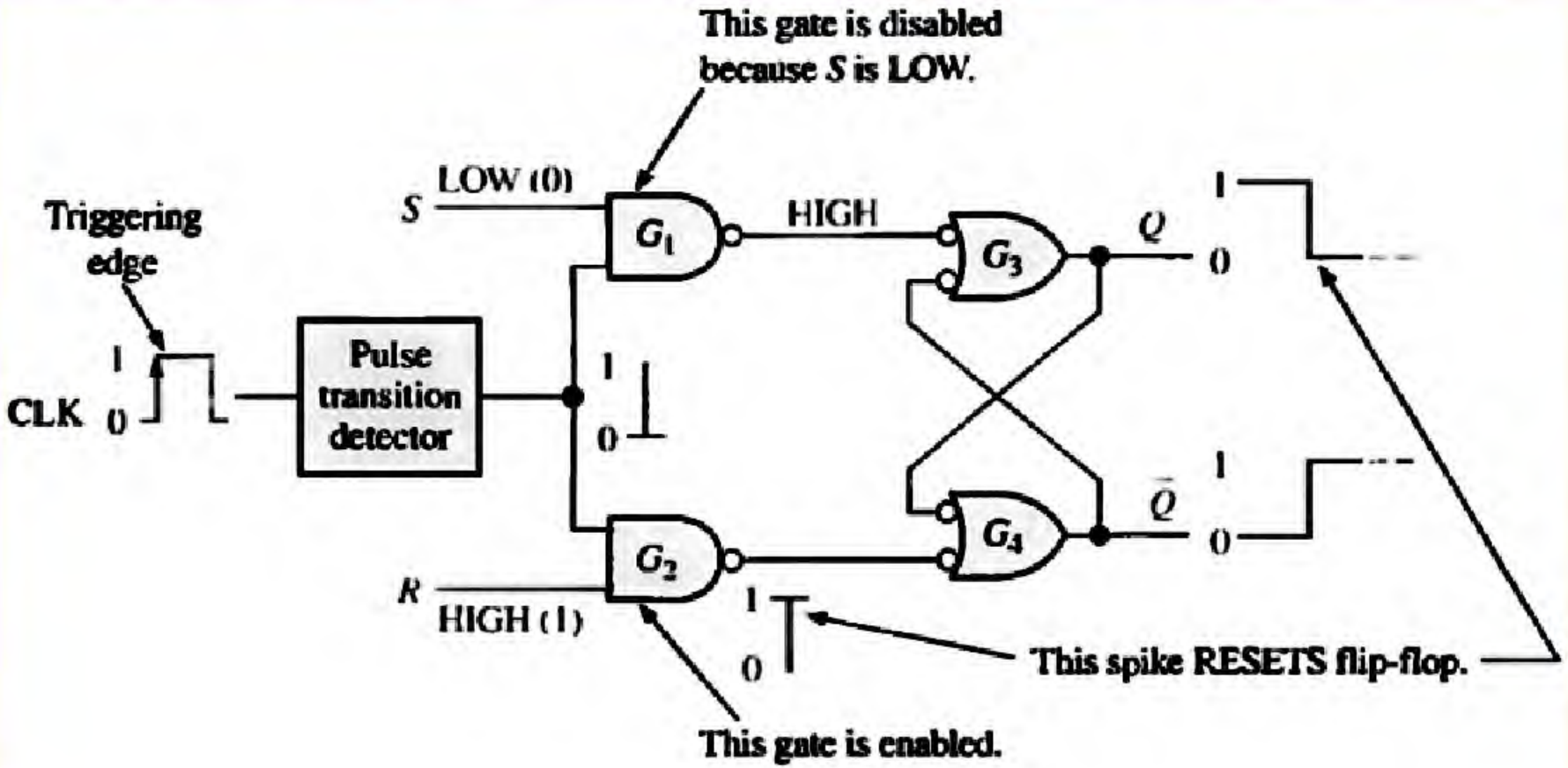
- ✓ The LOW on the Q output is coupled back into one input of gate G_4, making the $\overline{Q}$ output HIGH.
- ✓ Because Q is HIGH, both inputs to gate G_3 are HIGH (remember, the output of gate G_1 is HIGH), holding the Q output LOW.
- ✓ If a pulse is applied to the CLK input, the outputs of gates G_1 and G_2 remain HIGH because they are disabled by the LOWs on the S input and the R input; therefore, there is no change in the state of the flip-flop-it remains in the RESET state.

✓ Let's now make S HIGH, leave R LOW, and apply a clock pulse. Figure 1.9 illustrates the logic level transitions that take place within the flip-flop for this condition.



- ✓ Because the S input to gate G_1 is now HIGH, the output of gate G_1 goes LOW for a very short time (spike) when CLK goes HIGH, causing the Q output to go HIGH. Both inputs to gate G_4 are now HIGH (remember, gate G_2 output is HIGH because R is LOW), forcing the $\overline{Q}$ output LOW.
- ✓ This LOW on $\overline{Q}$ is coupled back into one input of gate G_3, ensuring that the Q output will remain HIGH. The flip-flop is now in the SET state.

✓ **Next, let's make S LOW and R HIGH and apply a clock pulse. Figure 1.10 illustrates the logic level transitions that occur within the flip-flop for this condition.**



- ✓ Because the R input is now HIGH, the positive-going edge of the clock produces a negative-going spike on the output of gate G_2 causing the $\overline{Q}$ output to go HIGH.
- ✓ Because of this HIGH on Q, both inputs to gate G_3 are now HIGH (remember, the output of gate G_1 is HIGH because of the LOW on S), forcing the Q output to go LOW.
- ✓ This LOW on Q is coupled back into one input of gate G_4, ensuring that Q will remain HIGH. The flip-flop is now in the RESET state.

- ✓ As with the gated latch, an invalid condition exists if a clock pulse occurs when both S and R are HIGH at the same time. This is the major drawback of the S-R flip-flop.

1.7-The Edge-Triggered D Flip-Flop.

- ✓ The D flip-flop is useful when a single data bit (1 or 0) is to be stored. The addition of an inverter to an S-R flip-flop creates a basic D flip-flop, as in Figure 1.11, where a positive edge-triggered type is shown.

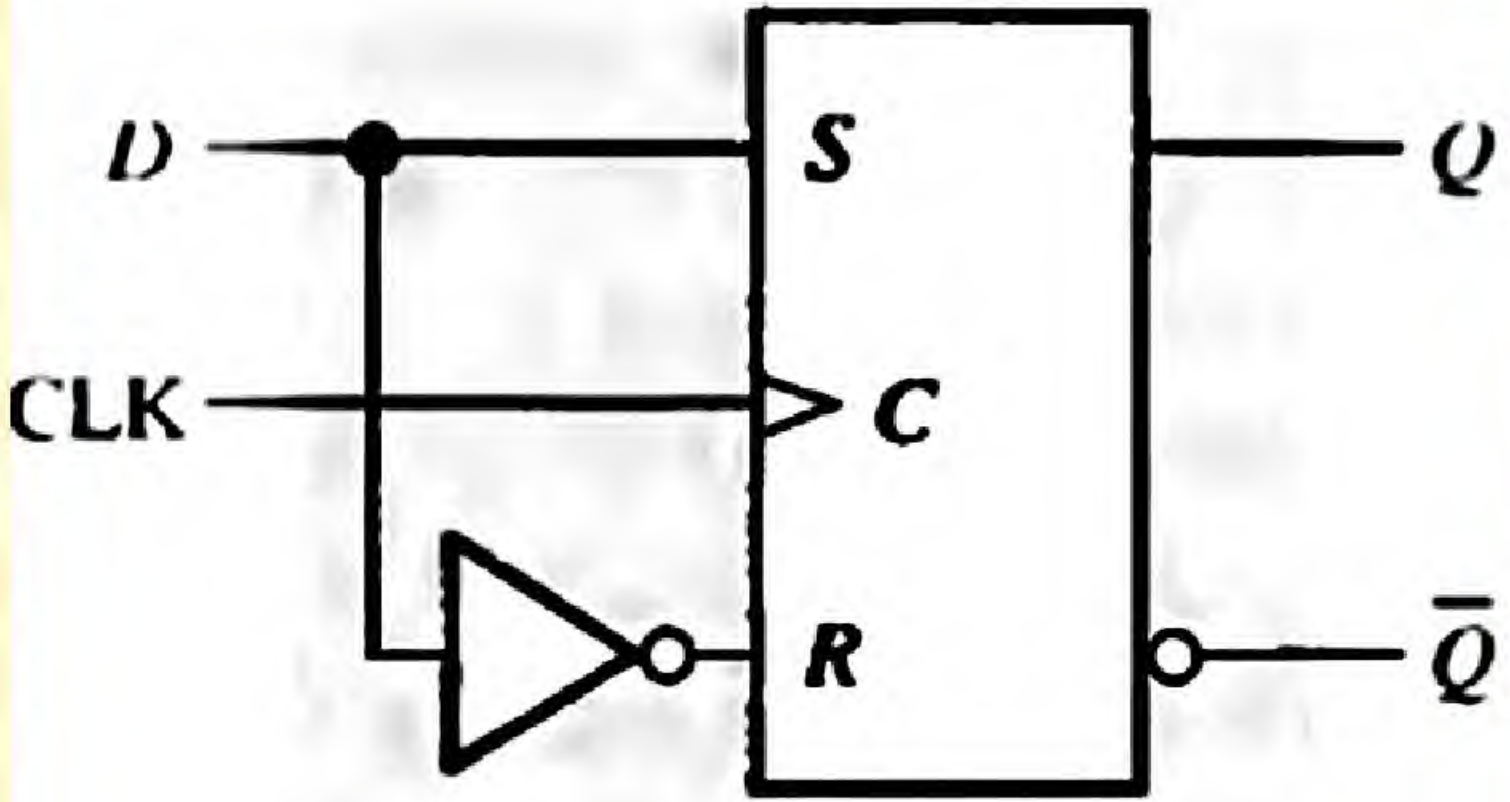


Figure 1.11

- ✓ Notice that the flip-flop in Figure 1.11 has only one input, the D input, in addition to the clock.
- ✓ If there is a HIGH on the D input when a clock pulse is applied, the flip-flop will SET, and the HIGH on the D input is stored by the flip-flop on the positive-going edge of the clock pulse.
- ✓ If there is a LOW on the D input when the clock pulse is applied, the flip-flop will RESET, and the LOW on the D input is stored by the flip-flop on the leading edge of the clock pulse.

- ✓ In the SET state the flip-flop is storing a 1, and in the RESET state it is storing a 0.
- ✓ The logical operation of the positive edge-triggered D flip-flop is summarized in Table 1-3.

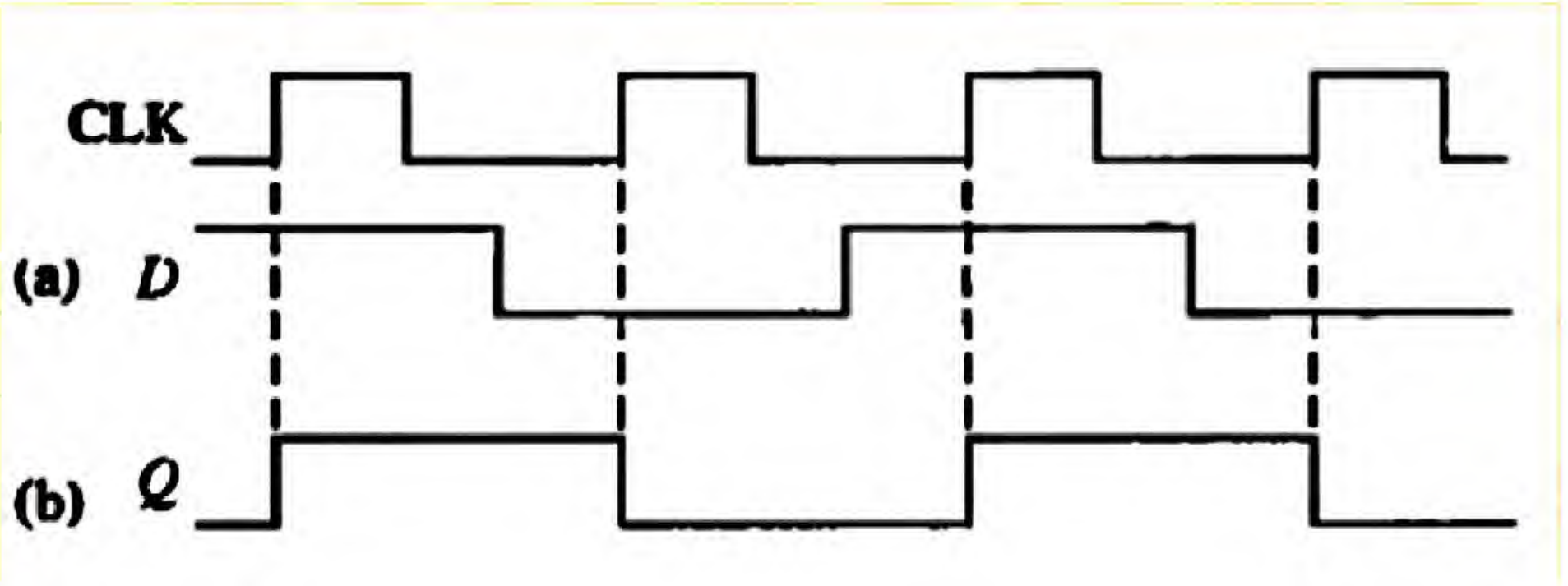
Truth table for a positive edge- triggered D flip-flop.

INPUTS		OUTPUTS		
D	CLK	Q	$\overline{Q}$	COMMENTS
1	↑	1	0	SET (stores a 1)
0	↑	0	1	RESET (stores a 0)

↑ = clock transition LOW to HIGH

- ✓ The operation of a negative edge-triggered device is, of course, the same, except that triggering occurs on the falling edge of the clock pulse.
- ✓ Remember, Q follows D at the active or triggering clock edge.

Example 1.5: Given the waveforms shown in the Figure for the D input and the clock, determine the Q output waveform if the flip-flop starts out RESET.


CLK
(a) D
(b) Q

1.8-The Edge-Triggered J-K Flip-Flop.

- ✓ The J-K flip-flop is versatile and is a widely used type of flip-flop.
- ✓ The functioning of the J-K flip-flop is identical to that of the S-R flip-flop in the SET RESET, and no-change conditions of operation.
- ✓ The difference is that the J-K flip-flop has no invalid state as does the S-R flip-flop. Figure 1.12 shows the basic internal logic for a positive edge-triggered J-K flip-flop.

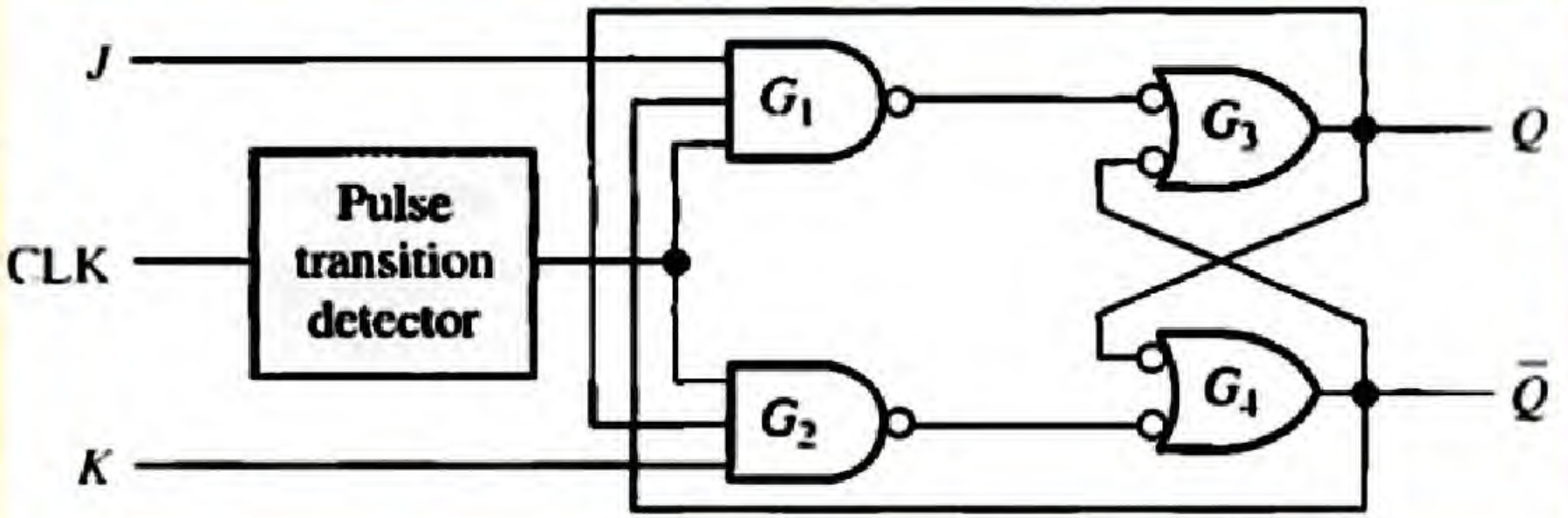


Figure 1.12

✓ It differs from the S-R edge triggered flip-flop in that the Q output is connected back to the input of gate G_2 and the $\overline{Q}$ output is connected back to the input of gate G_1.

- ✓ The two control inputs are labeled J and K in honor of Jack Kilby, who invented the integrated circuit.
- ✓ A J-K flip-flop can also be of the negative edge-triggered type, in which case the clock input is inverted.
- ✓ Table 1-4 summarizes the logical operation of the edge-triggered J-K flip-flop in truth table form.

Table(1-4)

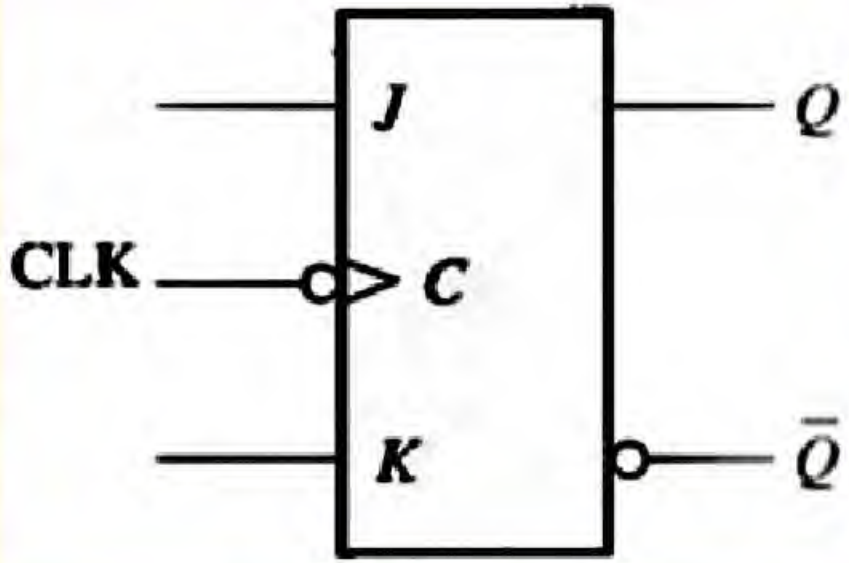
INPUTS			OUTPUTS		
J	K	CLK	Q	$\overline{Q}$	COMMENTS
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

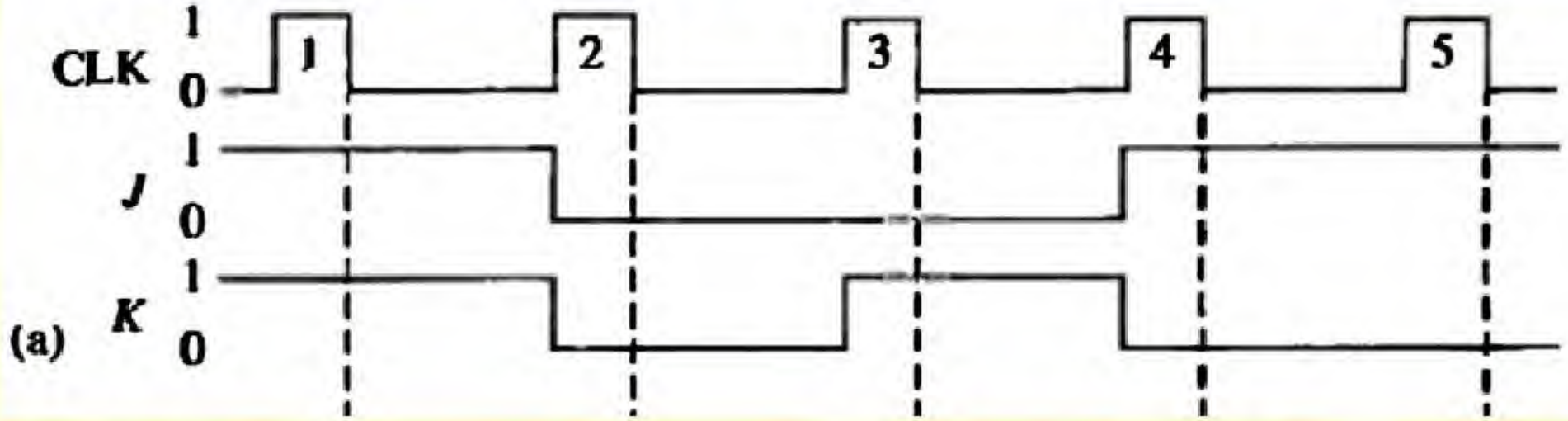
↑ = clock transition LOW to HIGH

Q_0 = output level prior to clock transition

- ✓ Notice that there is no invalid state as there is with an S-R flip-flop.
- ✓ The truth table for a negative edge-triggered device is identical except that it is triggered on the falling edge of the clock pulse.

Example 1.6: The waveforms shown in the Figure are applied to the J, K, and clock inputs as indicated. Determine the Q output, assuming that the flip-flop is initially RESET.





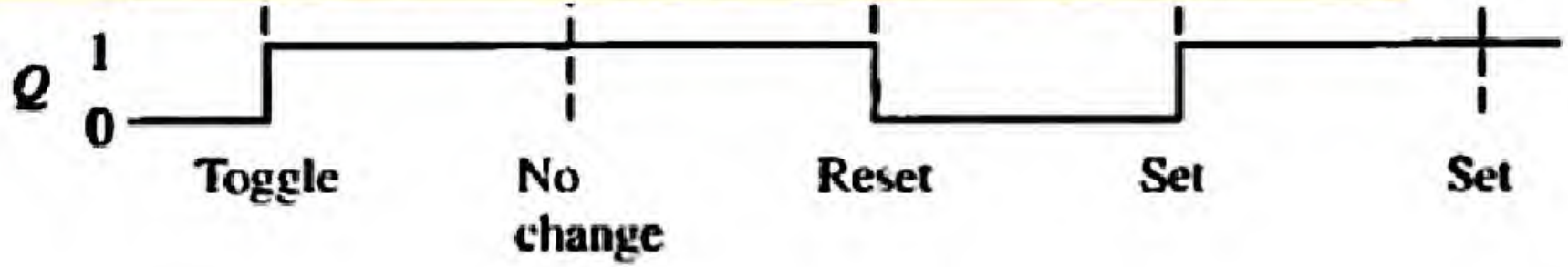
(a)

Solution.

State Table

CLK No.	J	K	State	Q	$\overline{Q}$
0	X	X	Reset	0	1
1	1	1	Toggle	1	0
2	0	0	NC	1	0
3	0	1	Reset	0	1
4	1	0	Set	1	0
5	1	0	Set	1	0

(b)



1. First, since this is a negative edge-triggered flip-flop, as indicated by the "bubble" at the clock input, the Q output will change only on the negative-going edge of the clock pulse.

2. At the first clock pulse, both J and K are HIGH; and because this is a toggle condition, Q goes HIGH.

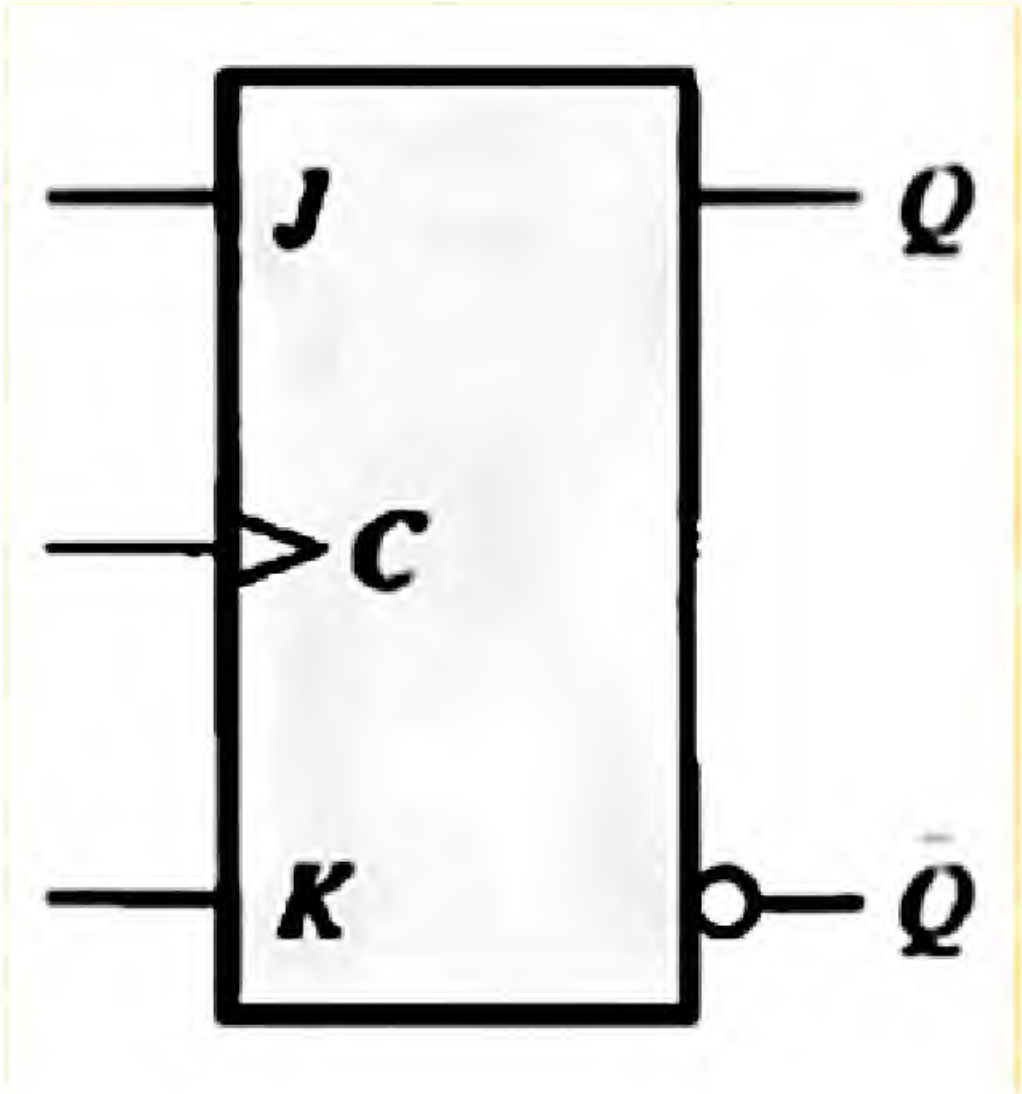
3. At clock pulse 2, a no-change condition exists on the inputs, keeping Q at a HIGH level.

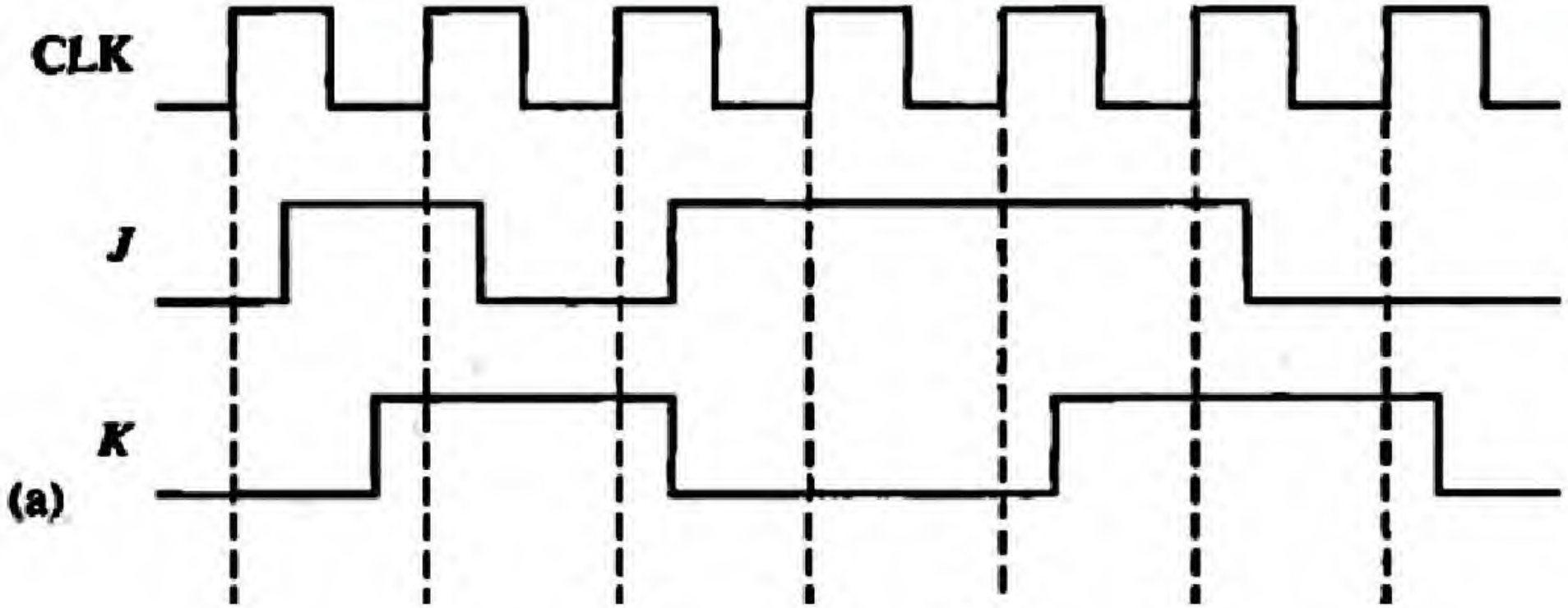
4. When clock pulse 3 occurs, J is LOW and K is HIGH, resulting in a RESET condition; Q goes LOW.

5. At clock pulse 4, J is HIGH and K is LOW, resulting in a SET condition; Q goes HIGH.

6. A SET condition still exists on J and K when clock pulse 5 occurs, so Q will remain HIGH.

Example 1.7: The waveforms shown in the Figure are applied to the flip-flop. Determine the Q output, starting in the RESET state.

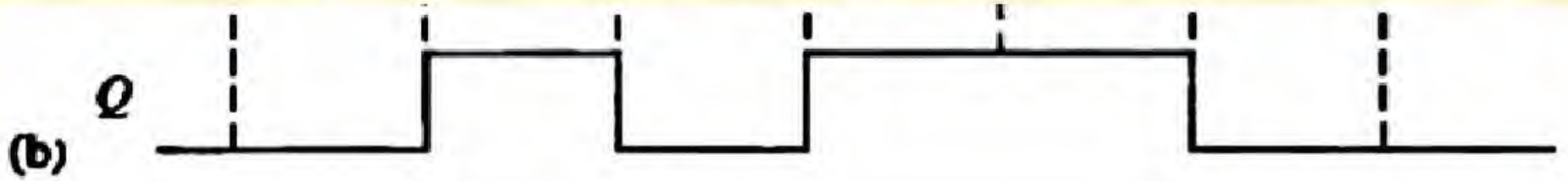

J
C
K
Q
$\bar{Q}$


CLK
J
K
(a)

State Table

CLK No.	J	K	State	Q	$\overline{Q}$
0	X	X	Reset	0	1
1	0	0	NC	0	1
2	1	1	Toggle	1	0
3	0	1	Reset	0	1
4	1	0	Set	1	0
5	1	0	Set	1	0
6	1	1	Toggle	0	1
7	0	1	Reset	0	1

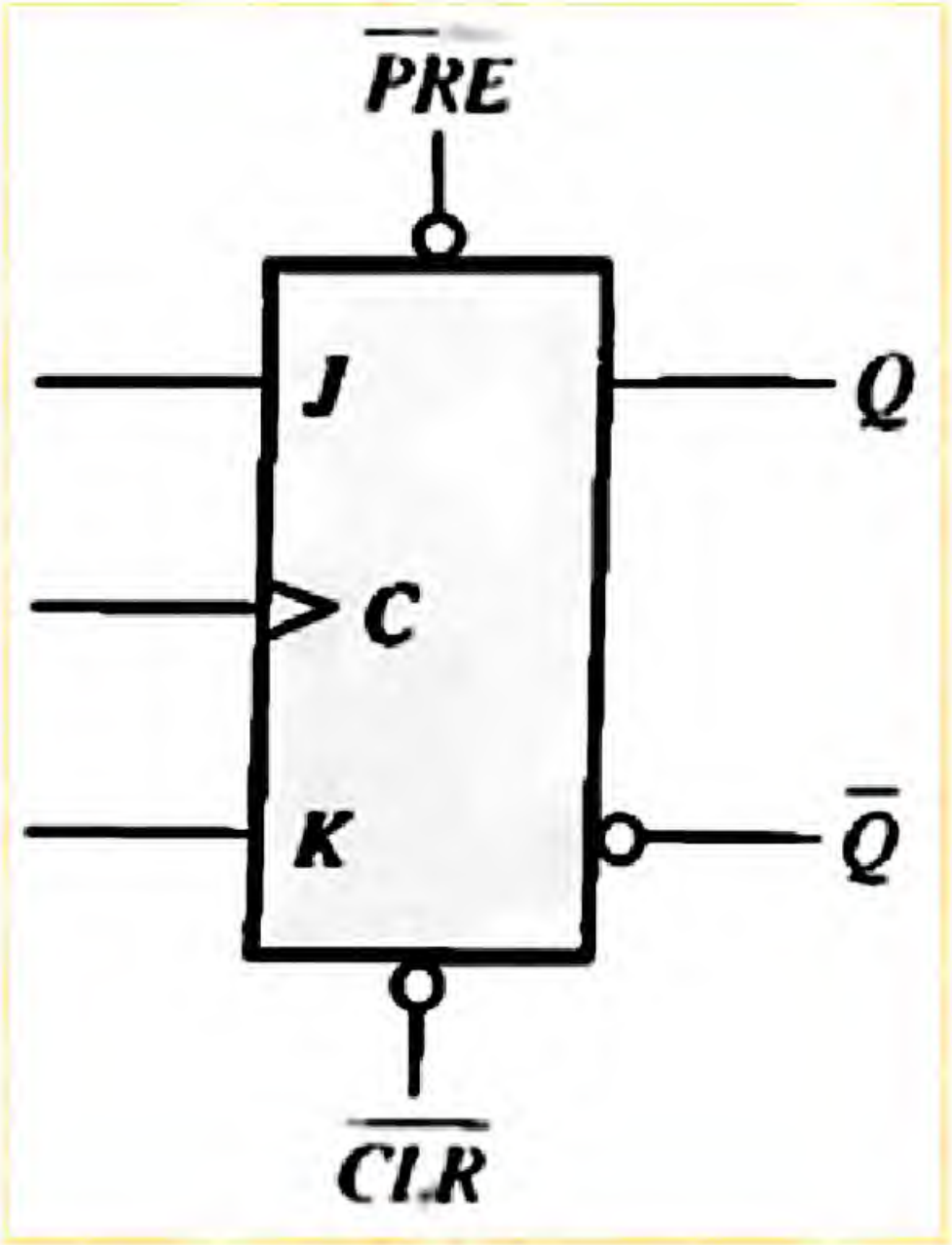
- ✓ The Q output assumes the state determined by the states of the J and K inputs at the positive-going edge (triggering edge) of the clock pulse.
- ✓ A change in J or K after the triggering edge of the clock has no effect on the output, as shown in the Figure.



1.9-Asynchronous Preset and Clear Inputs

- ✓ For the flip-flops just discussed, the S-R, D. and J-K inputs are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse: that is the data are transferred synchronously with the clock.
- ✓ Most integrated circuit flip-flops also have asynchronous inputs. These are inputs that affect the state of the flip-flop independent of the clock.

- ✓ They are normally labeled preset (PRE) and clear (CLR), or direct set (S_D) and direct reset (R_D) by some manufacturers.
- ✓ An active level on the PRESET input will SET the flip-flop, and an active level on the CLEAR input will RESET it. A logic symbol for a J-K flip-flop with PRESET and CLEAR inputs is shown in Figure 1.13.


$\overline{PRE}$
J
C
K
Q
$\overline{Q}$
$\overline{CLR}$

- ✓ These inputs are active-LOW, as indicated by the bubbles. These PRESET and CLEAR inputs must both be kept HIGH for synchronous operation.
- ✓ Figure 1.14 shows the logic diagram for an edge-triggered J-K flip-flop with active-LOW PRESET (PRE) and CLEAR (CLR) inputs.

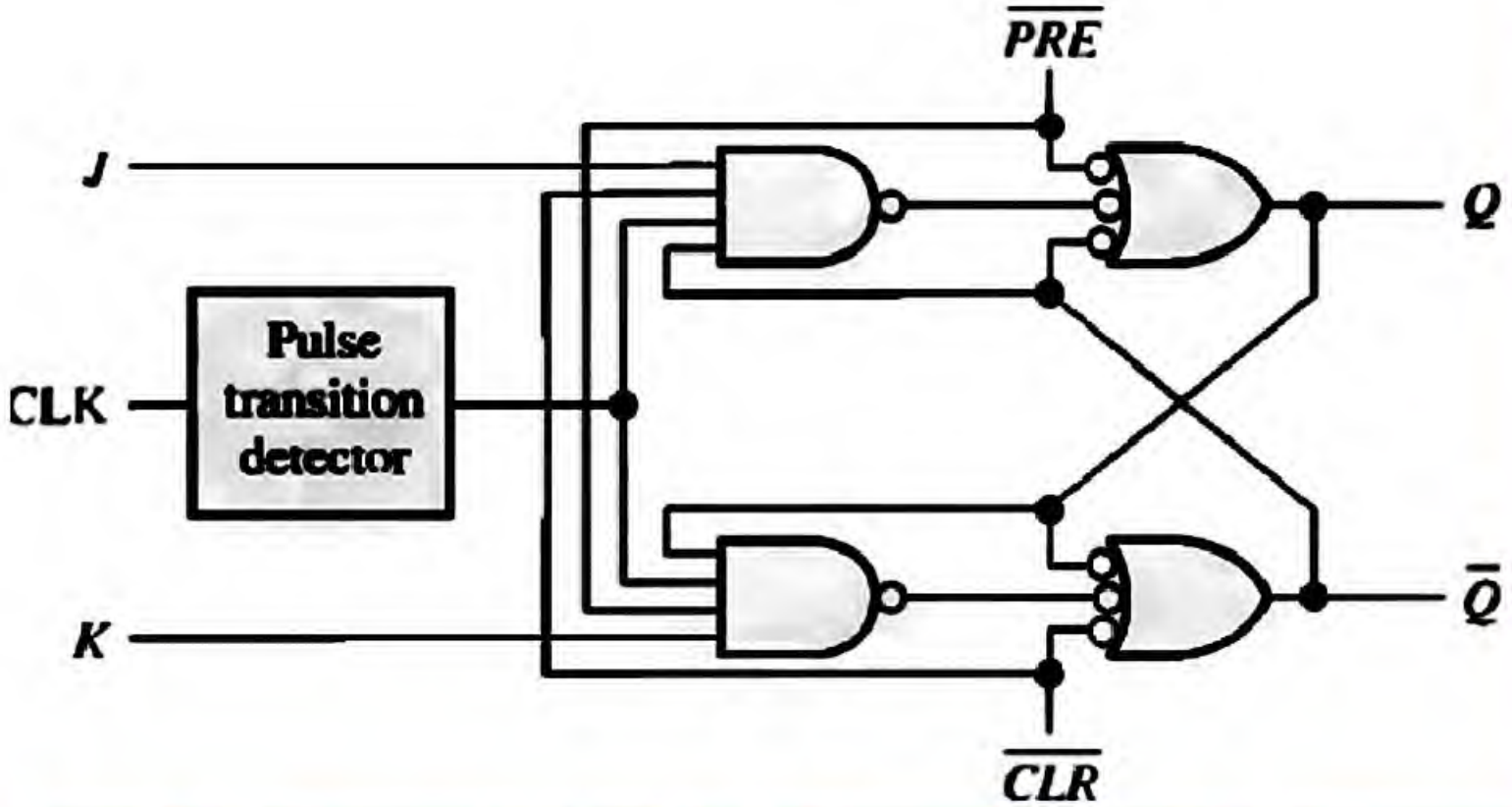


Figure 1.14

✓ This figure illustrates basically how these inputs work. As you can see, they may connect so that they override the effect of the synchronous inputs, J, K, and the clock.